1. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

2. A method according to Claim 1, further comprising forming a liner upon a sidewall of each said isolation trench.

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3. A method according to Claim 2, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

4. A method according to Claim 2, wherein forming said liner upon said sidewall of said isolation trench comprises deposition of a composition of matter.

5. A method according to Claim 1, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

6. A method according to Claim 1, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

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7. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein:

material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

said conformal layer and said spacers form said upper surface for each said isolation trench, each said upper surface being formed from said conformal layer and said spacer and being situated above said pad oxide layer; and

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said first dielectric layer is in contact with at least a pair of said spacers and said pad oxide layer.

8. A method according to Claim 7, further comprising:

removing said pad oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

9. A method according to Claim 7, wherein said upper surface for each said isolation trench is formed in an etch process using an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from of about 1:1 to about 2:1.

10. A method according to Claim 9, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

11. A method according to Claim 7, wherein said upper surface for each said isolation trench is formed by the steps comprising:

chemical mechanical planarization, wherein said conformal layer, said spacers, and said first dielectric layer form a planar first upper surface; and

an etch that forms a second upper surface, said second upper surface being situated above said pad oxide layer.

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12. A method according to Claim 11, wherein said etch uses an etch recipe that etches said first dielectric layer faster than said conformal layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

13. A method according to Claim 11, wherein said ratio in a range from about 1.3:1 to about 1.7:1.

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14. A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding electrically active region below the termination of said each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

filling each said isolation trench with a second silicon dioxide layer, said second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers; and

selectively removing said second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said pad oxide layer, wherein material that

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is electrically insulative extends continuously between and within said plurality of isolation trenches.

15. A method according to Claim 14, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

16. A method according to Claim 14, wherein said liner is composed of silicon nitride.

17. A method according to Claim 15, further comprising:

removing said oxide layer upon a portion of a surface of said semiconductor substrate; and

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate.

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18. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein planarizing the conformal third layer to form therefrom said upper surface for each said isolation trench that is co-planar to the other said upper surfaces

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further comprises planarizing said conformal third layer and each said spacer to form therefrom said co-planar upper surfaces.

19. A method according to Claim 18, wherein said upper surface for each said isolation trench is formed by chemical mechanical planarization.

20. A method according to Claim 18, further comprising forming a doped region below the termination of each said isolation trench within said semiconductor substrate.

21. A method according to Claim 18 , further comprising, prior to filling each said isolation trench with said conformal third layer, forming a liner upon a sidewall of each said isolation trench that extends from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate, and wherein said conformal third layer is composed of an electrically conductive material.

22. A method according to Claim 21, wherein said a liner is a thermally grown oxide of said semiconductor substrate.

23. A method according to Claim 21, wherein forming said liner upon said sidewall of each said isolation trench comprises deposition of a composition of matter.

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24. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

wherein said upper surface for each said isolation trench is formed from said conformal third layer, said spacers, and said first dielectric layer.

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25. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate;

forming a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers; and

selectively removing said third layer, said spacers and said layer composed of polysilicon to form a portion of at least one of said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

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26. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer by an etch using an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from of about 1:1 to about 2:1 to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

27. A method according to Claim 26, wherein said ratio is in a range from about 1.3:1 to about 1.7:1.

28. A method of a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a first dielectric layer upon said polysilicon layer;

selectively removing said first dielectric layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer conformally over said oxide layer, said polysilicon layer, and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is upon said oxide layer, is in contact with both said polysilicon layer and said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

filling each said isolation trench with a conformal third layer, said conformal third layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing the conformal third layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces;

chemical mechanical planarization of said conformal third layer, said spacers, and said first dielectric layer to form a planar first upper surface; and

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an etch that forms a planar second upper surface, said second upper surface being situated above said oxide layer;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

29. A method according to Claim 28, wherein said etch uses an etch recipe that etches said first dielectric layer faster than said conformal third layer and said spacers by a ratio in a range from about 1:1 to about 2:1.

30. A method of forming and filling an isolation trench according to Claim 28, wherein said ratio in a range from about 1.3:1 to about 1.7:1.

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31. A method of forming a microelectronic structure, the method comprising:

forming a pad oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon said oxide layer;

forming a silicon nitride layer upon said polysilicon layer;

selectively removing said silicon nitride layer and said polysilicon layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is in contact with said silicon nitride layer and said polysilicon layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas;

forming a corresponding doped region below the termination of each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, each said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

filling each said isolation trench with a second layer, said second layer extending above said oxide layer in contact with a corresponding pair of said spacers; and

planarizing said second layer and each of said spacers to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and is situated above said oxide layer;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

32. A method according to Claim 31, wherein each said liner is a thermally grown oxide of said semiconductor substrate, and wherein said second layer is composed on an electrically conductive material.

33. A method according to Claim 31, wherein each said liner is composed of silicon nitride, and wherein said second layer is composed on an electrically conductive material.

34. A method according to Claim 31, further comprising:

exposing said oxide layer upon a portion of a surface of said semiconductor substrate;

forming a gate oxide layer upon said portion of said surface of said semiconductor substrate; and

forming a layer composed of polysilicon upon said gate oxide layer in contact with a pair of said spacers, and

selectively removing said layer composed of polysilicon to form a portion of at least one of said upper surfaces.

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35. A method for a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said

isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer.

36. The method as defined in Claim 35, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each said isolation trench.

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37. The method as defined in Claim 36, wherein the doped trench bottom has a width, each said the isolation trench has a width, and the width of each said doped trench bottom is greater than the width of the respective isolation trench.

38. A method for a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said

isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; and

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer.

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39. The method as defined in Claim 38, further comprising:

doping the semiconductor substrate with a dopant having a first conductivity type; and

doping the semiconductor substrate below each said isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of said isolation trenches.

40. The method as defined in Claim 39, wherein:

the doped trench bottom has a width;

each said isolation trench has a width; and

the width of each said doped trench bottom is greater than the width of the respective isolation trench.

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41. A method of a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface;

forming first and second isolation trenches each:

extending into and being defined by the semiconductor substrate;

having an opening thereto at the top surface of the semiconductor substrate; and

extending below and being centered between a pair of spacers situated above the top surface of the semiconductor substrate;

and wherein:

an electrically insulative material extends continuously between and within the first and second isolation trenches; and

a planar surface begins at the first isolation trench and extends continuously to the second isolation trench.

42. A method for a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate

adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

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forming a planar upper surface from said second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer.

43. A method of a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said

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first spacer of said second isolation structure is situated on a side of said first isolation trench;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

forming a planar upper surface formed from said second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer.

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